#14

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Chandrakant B. Patel et al

Appln. No. 08/266,753 Group Art Unit: 2602

Filed: June 28, 1994 Examiner: V. Kostak

For: RADIO RECEIVER FOR RECEIVING BOTH VSB AND QAM DIGITAL HDTV SIGNALS

ATTN: OFFICE OF ASSISTANT COMMISSIONER OF PATENTS
CRYSTAL PARK 1, ROOM 520

PETITION UNDER § 37 CFR 1.313
TO WITHDRAW A PATENT FROM ISSUE

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

On January 16, 1996, the issue fee was paid in the referenced case. Subsequently, it was discovered by the Applicants that the present Figure 7 in the application as allowed (Exhibit A) is incorrect and does not correspond at all with the text of the specification at pages 34 and 35 of the application (Exhibit B). A correct copy of the Figure is attached (Exhibit C). While the improper figure was submitted by the Applicant in the original application, the failure to detect the error during prosecution of the application was the result of a mistake on the part of the Office. In order to permit a correction of this error, and the substitution of the proper figure, withdrawal from issue pursuant to Rule 313 is appropriate.

Correction of the error is necessary in order to ensure that the application drawings fully correspond to the description in the specification. At present, the referenced application contains a description in the specification (at pages 34 and 35) that does not have a corresponding drawing and a drawing (Fig. 7) that has no corresponding text in the specification. Correction under these circumstances is necessary in order to provide the public with an accurate description of the disclosed invention.

Correction of the error would be accomplished through the accompanying Amendment Under 37 CFR 1.312, in which the original Figure 7 is deleted and the new Figure 7 is substituted. A petition as required by Rule 312 (b) accompanies the amendment.

08/243,480 filed May 19, 1994 and (4) the copending application SN. 08/243,480 referenced above contains a disclosure at pages 31 and 32 and a corresponding Figure 14 (Exhibit E) that are virtually identical (but for reference numbers) to the original text at pages 34 and 35 of the present application and the substitute Figure 7 submitted herewith as Exhibits B and C, respectively.

Correction of the error by substitution of the new drawing is proper and would not involve the addition of new matter because (1) the above referenced application includes at pages 34 and 35 a clear and detailed description of the content of the correct Figure 7, (2) the above referenced application includes at pages 35 and 36 and in original Figure 8 a description of a modification of the circuit described at pages 34 and 35 that should have been illustrated in Figure 7, such description having the effect of leading one of ordinary skill to construct a proper illustration of the circuit as presented in substitute Figure 7; (3) the present application expressly incorporates by reference, at pages 4 and 5 of the application (Exhibit D), the content of commonly assigned and copending application SN. 08/243,480 filed May 19, 1994 and (4) the copending application SN. 08/243,480 referenced above contains a disclosure at pages 31 and 32 and a corresponding Figure 14

(Exhibit E) that are virtually identical (but for reference numbers) to the original text at pages 34 and 35 of the present application and the substitute Figure 7 submitted herewith as Exhibits B and C, respectively.

In the event that the Commissioner concludes that the error was not due to a mistake of the Office and that relief is not available to Applicants under 37 CFR 1.313(b), Applicants authorizes the payment of the appropriate fee set forth in 37 CFR 1.17(I)(1) should be charged to Deposit Account No. 19-4880. A duplicate copy of this Paper is enclosed.

Respectfully submitted,

SUGHRUE, MION, ZINN,
MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3202
(202) 293-7060

Alan J. Kasper
Registration No. 25,426

Date: April 5, 1996

PATENT APPLICATION

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Appln. No. 08/266,753 Group Art Unit: 2602

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CRYSTAL PARK 1, ROOM 520

PETITION UNDER § 37 CFR 1.312
FOR AMENDMENT AFTER PAYMENT OF ISSUE FEE

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

On January 16, 1996, the issue fee was paid in the referenced case. Subsequently, in February 1996, it was discovered by one of the Applicants, Allen Limberg that the present Figure 7 in the application as allowed (Exhibit A) is incorrect and does not correspond at all with the text of the specification at pages 34 and 35 of the application (Exhibit B). A correct copy of the Figure was prepared and is attached (Exhibit C). It appears that at no time during the prosecution of the application prior to the payment of the issue fee did the Examiner, the Applicants or the Applicantss' representative discover that original Figure 7 did not correspond to the related text of the specification at pages 34 and 35. Accordingly, no earlier amendment to the drawings to correct the error was possible, particularly an amendment prior to the payment of the issue fee.

Correction of the error is necessary in order to ensure that the application drawings fully correspond to the description in the specification. At present, the referenced application contains a description in the specification (at pages 34 and 35) that does not have a corresponding drawing and a drawing (Fig. 7) that has no corresponding text in the specification. Correction under these circumstances is necessary in order to provide the public with an accurate description of the disclosed invention.

Correction of the error would be accomplished through the accompanying Amendment Under 37 CFR 1.312, in which the original Figure 7 is deleted and the new Figure 7 is substituted.

Correction of the error by substitution of the new drawing is proper and would not involve the addition of new matter because (1) the above referenced application includes at pages 34 and 35 a clear and detailed description of the content of the correct Figure 7, (2) the above referenced application includes at pages 35 and 36 and in original Figure 8 a description of a modification of the circuit described at pages 34 and 35 that should have been illustrated in Figure 7, such description having the effect of leading one of ordinary skill to construct a proper illustration of the circuit as presented in substitute Figure 7; (3) the present application expressly incorporates by reference, at pages 4 and 5 of the application (Exhibit D), the content of commonly assigned and copending application SN. 08/243,480 filed May 19, 1994 and (4) the copending application SN. 08/243,480 referenced above contains a disclosure at pages 31 and 32 and a corresponding Figure 14 (Exhibit E) that are virtually identical (but for reference numbers and a corrected sign at summer 126) to the original text at pages 34 and 35 of the present application and the substitute Figure 7 submitted herewith as Exhibits B and C, respectively.

Applicants authorizes the payment of the appropriate fee set forth in 37 CFR 1.17(I)(1) should be charged to Deposit Account No. 19-4880. A duplicate copy of this Paper is enclosed.

Respectfully submitted,

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EXHIBIT A

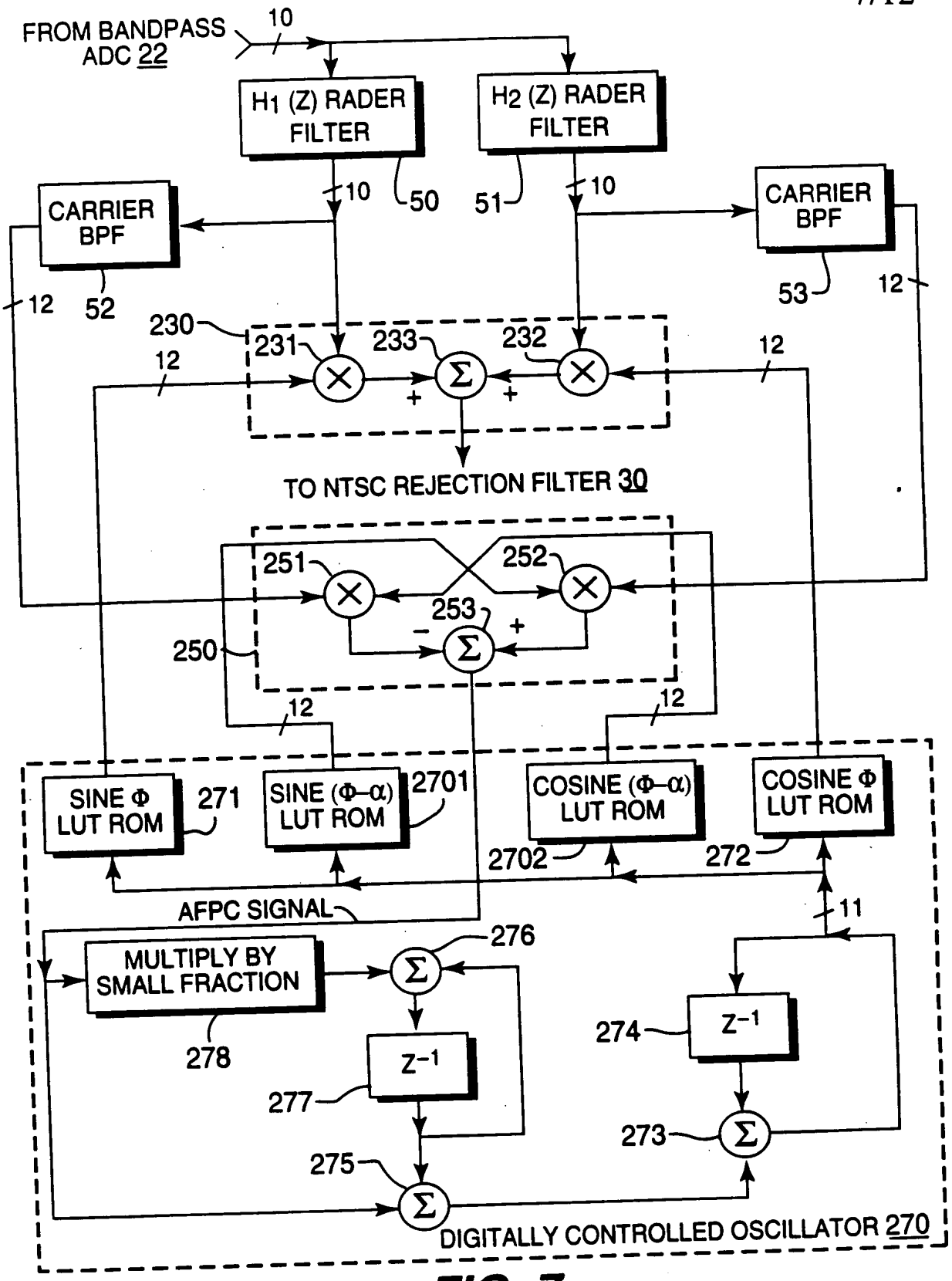

FIG. 7

improvements in complex synchronous detection carried out on digitized bandpass signals. Rader replaces the Hilbert-transform FIR filter and the compensating-delay FIR filter of Rice and Wu with a pair of all-pass digital filters designed based on Jacobian elliptic functions and exhibiting a constant $\pi/2$ difference in phase response for the digitized bandpass signals. A preferred pair of such all-pass digital filters has the following system functions:

$$H_1(z) = z^{-1}(z^{-2} - a^2) / (1 - a^2 z^{-2}) \quad a^2 = 0.5846832$$

$$H_2(z) = -(z^{-2} - b^2) / (1 - b^2 z^{-2}) \quad b^2 = 0.1380250$$

Rader describes filter configurations which require only two multiplications, one by a^2 and one by b^2.

FIGURE 7 shows an alternative form that the circuitry **24** can take, which comprises a pair of all-pass digital filters **80** and **90** of a type described by C. M. Rader and designed based on Jacobian elliptic functions. The filters **80** and **90** exhibit a constant $\pi/2$ difference in phase response for digitized bandpass signals. Since oversampled real samples better provide for symbol synchronization when synchrodyning VSB signals, the inventors prefer not to use the all-pass filters described by Rader that exploit sub-sampling to provide further reductions in the delay network circuitry.

The construction of the filter **80**, which provides the system function $H_1(z) = z^{-1}(z^{-2} - a^2) / (1 - a^2 z^{-2})$, where $a^2 = 0.5846832$ in decimal arithmetic, is shown in FIGURE 7 to be as follows. The samples from the ADC **22** are delayed by one ADC sample clock duration in a clocked delay element **88** for application to a node **89**. The signal at node **89** is further delayed by two ADC sample clock durations in cascaded clocked delay elements **81** and **82**, for application as its first summand signal to a digital adder **83**. The sum output signal of the adder **83** provides the real response from the filter **80**. The sum output signal of the adder **83** is delayed by two ADC sample clock durations in cascaded clocked delay elements **84** and **85**, for application as minuend input signal to a digital subtractor **86** that receives

the signal at node **89** as its subtrahend input signal. The resulting difference output signal from the digital subtractor **86** is supplied as multiplier input signal to a digital multiplier **87** for multiplying an a^2 multiplicand signal, using a binary arithmetic. The resulting product output signal is applied to the digital adder **83** as its second summand signal.

The construction of the filter **90**, which provides the system function $H_2(z) = -(z^{-2} - b^2) / (1 - b^2 z^{-2})$, where $b^2 = 0.1380250$ in decimal arithmetic, is shown in FIGURE 7 to be as follows. The samples from the ADC **22** are delayed by two ADC sample clock durations in cascaded clocked delay elements **91** and **92**, for application as its first summand signal to a digital adder **93**. The sum output signal of the adder **93** provides the imaginary response from the filter **90**. The sum output signal of the adder **93** is delayed by two ADC sample clock durations in cascaded clocked delay elements **94** and **95**, for application to a digital adder **96** as its second summand signa, which receives the samples from the ADC **22** as its subtrahend input signal. The resulting sum output signal from the digital adder **96** is supplied as multiplier input signal to a digital multiplier **97** for multiplying a b^2 multiplicand signal, using a binary arithmetic. The resulting product output signal is applied to the digital adder **93** as its second summand signal.

FIGURE 8 shows a complex-signal filter resulting from modifying the FIGURE 7 complex-signal filter as follows. The position of the clocked delay element **88** is shifted so as to delay the sum output signal of the adder **83**, rather than to delay the digital output signal of the ADC **22**, and the digital output signal of the ADC **22** is applied to the node **89** without delay, thereby to cause real response to be provided at the output port of the shifted-in-position clocked delay element **88**. The real response provided at the output port of the shifted-in-position clocked delay element **81** is the same as the response provided at the output port of the clocked delay element **84**. So, the real response is provided from the output port of the clocked delay element **84** instead of from the output port of the

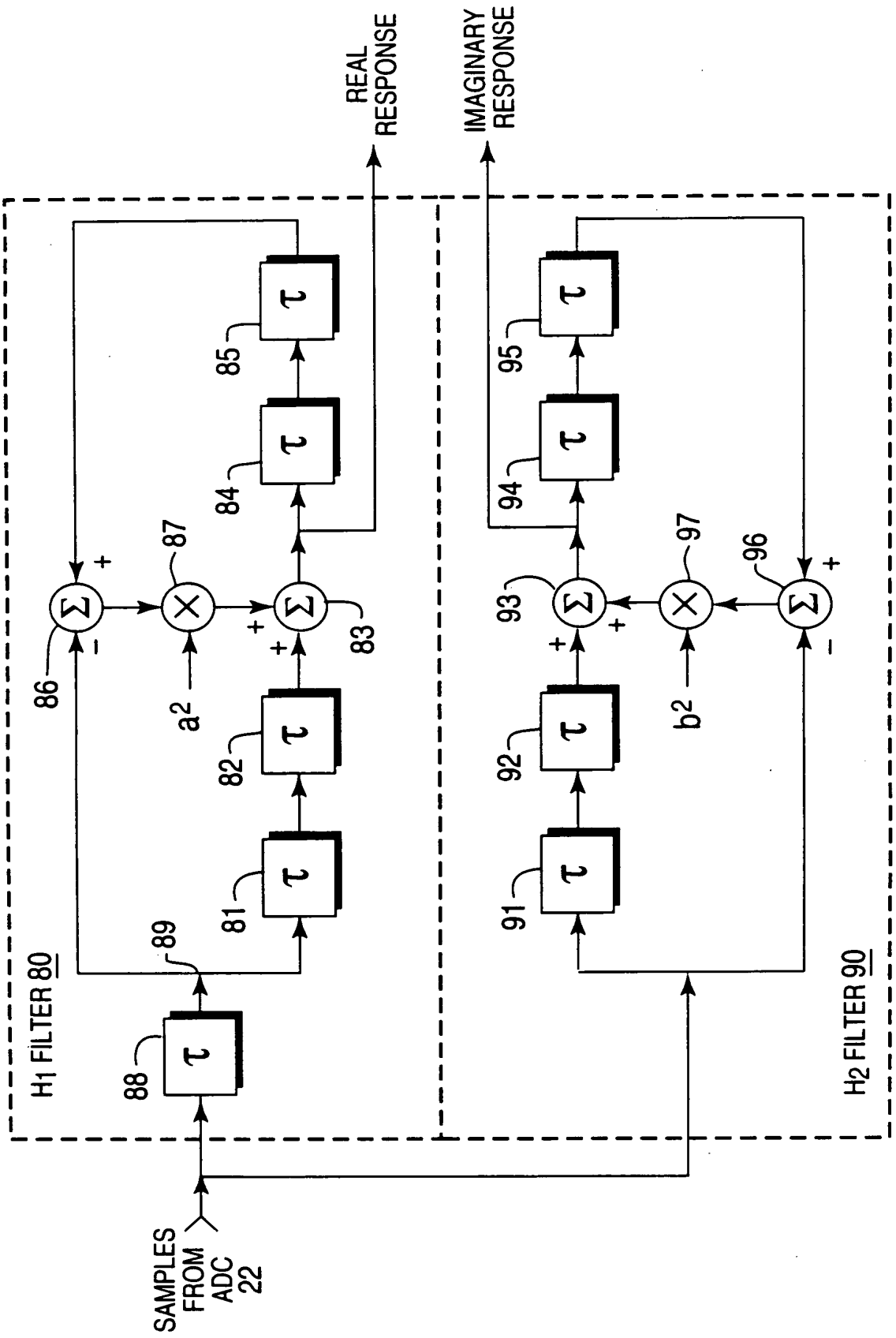
REAL RESPONSE
IMAGINARY RESPONSE
SAMPLES FROM ADC 22
H1 FILTER 80
H2 FILTER 90
88
89
81
82
83
84
85
86
87
a2
91
92
93
94
95
96
97
b2
τ
Σ
+
-
×

FIG. 7

and the methods of locking the frequency and phase of symbol decoding differ in the VSB and QAM HDTV receivers.

The inventors point out that these types of known digital HDTV signal radio receiver present some problem in the design of the tuner portion of the receiver because the respective carrier frequencies of VSB HDTV signals and of QAM HDTV signals are not the same as each other. The carrier frequency of a QAM HDTV signal is at mid-channel of the transmission frequencies. The carrier frequency of a VSB HDTV signal is 2.375 MHz below mid-channel frequency. Accordingly, the third local oscillations of fixed frequency, which are used for synchrodyning to baseband, must be of different frequency when synchrodyning VSB HDTV signals to baseband than when synchrodyning QAM HDTV signals to baseband. The 2.375 MHz difference in frequency is larger than that which is readily accommodated by applying automatic frequency and phase control to the third local oscillator. A third oscillator that can switchably select between two frequency-stabilizing crystals is a practical necessity. In such an arrangement, of course, alterations in the tuner circuitry are involved with arranging for the automatic selection of the appropriate mode of reception for the HDTV transmission currently being received. The radio-frequency switching that must be done reduces the reliability of the tuner. The RF switching and the additional frequency-stabilizing crystal for the third oscillator increase the cost of the tuner appreciably.

Radio receivers for receiving VSB HDTV signals, in which receiver the third mixer output signal is a final intermediate-frequency signal somewhere in the 1 - 8 MHz frequency range rather than at baseband, are described by the inventors in the U. S. patent applications listed below, incorporated by reference herein, and commonly assigned herewith:

Serial No. 08/237,896 filed 4 May 1994 and entitled **DIGITAL VSB DETECTOR WITH BANDPASS PHASE TRACKER, AS FOR INCLUSION IN AN**

HDTV RECEIVER;

Serial No. 08/243,480 filed 19 May 1994 and entitled **DIGITAL VSB DETECTOR WITH BANDPASS PHASE TRACKER USING RADER FILTERS, AS FOR USE IN AN HDTV RECEIVER**; and

Serial No. 08/247,753 filed 23 May 1994 and entitled **DIGITAL VSB DETECTOR WITH FINAL I-F CARRIER AT SUBMULTIPLE OF SYMBOL RATE, AS FOR HDTV RECEIVER.**

The final IF signal is digitized and the synchrodyne procedures are carried out in the digital regime. Radio receivers that receive QAM signals, convert them to a final IF signal just above baseband, and synchrodyne the final IF signal in the digital regime are known; and such receivers can be adapted for receiving HDTV signals, it is believed to be evident at this time to a television receiver designer of ordinary skill in the art. In radio receivers that are to have the capability of receiving digital HDTV signals no matter whether they are transmitted using VSB or QAM, the inventors point out, conversion of the signals to final IF signals just above baseband permits the frequency of the oscillations of the third local oscillator to remain the same no matter whether VSB or QAM transmissions are being received. The differences in carrier frequency location within the channel can be accommodated in the synchrodyning procedures carried out in the digital regime.

Summary of the Invention

The invention is embodied in a radio receiver for receiving a selected one of digital HDTV signals each including symbol codes descriptive of digital signals, irrespective of whether said selected HDTV signal is a quadrature-amplitude-modulation (QAM) signal or is a vestigial sideband (VSB) signal including a pilot carrier having an amplitude related to signal levels in said symbol codes thereof. A tuner within the receiver includes elements for selecting one of channels at different locations in a frequency band used for transmitting

filter **43**, for generating products that define boundary values for the amplitude range bins in the quantizer **84**. These boundary values are applied to digital comparators in the quantizer **84** for having the quantizer **84** input signal compared against these values. The continuous availability of the pilot carrier, which has substantial signal energy, facilitates rapid tracking of the decision levels in the quantizer **84** with changes in VSB signal strength.

FIGURE 14 is a detailed block schematic diagram of a complex-signal filter. The FIGURE 16 filter includes a pair of all-pass digital filters **110** and **120** designed based on Jacobian elliptic functions and exhibiting a constant $\pi/2$ difference in phase response for the digitized bandpass signals, as described by C. M. Rader. The filters **150** and **151** of FIGURE 6, 7, 8 or 9 can be constructed like filters **110** and **120**. So can the filters **157** and **158** of FIGURE 7. Since oversampled real samples better provide for the proper functioning of the mean-square-error gradient detection filter **90** in the symbol synchronizer **3**, in their digital circuitry for synchrodyning VSB signals, the inventors prefer not to use other all-pass filters that Rader describes which exploit sub-sampling to provide further reductions in the delay network circuitry.

The construction of the filter **110**, which provides the system function $H_1(z) = z^{-1} (z^{-2} - a^2) / (1 - a^2 z^{-2})$, where $a^2 = 0.5846832$ in decimal arithmetic, is shown in FIGURE 16 to be as follows. The samples from the ADC **22** are delayed by one ADC sample clock duration in a clocked delay element **118** for application to a node **119**. The signal at node **119** is further delayed by two ADC sample clock durations in cascaded clocked delay elements **111** and **112**, for application as its first summand signal to a digital adder **113**. The sum output signal of the adder **113** provides the real response from the filter **110**. The sum output signal of the adder **113** is delayed by two ADC sample clock durations in cascaded clocked delay elements **114** and **115**, for application as minuend input signal to a digital subtractor **116** that receives the signal at node **119** as its subtrahend input signal. The resulting difference output

signal from the digital subtractor **116** is supplied as multiplier input signal to a digital multiplier **117** for multiplying an a^2 multiplicand signal, using a binary arithmetic. The resulting product output signal is applied to the digital adder **113** as its second summand signal.

The construction of the filter **120**, which provides the system function $H_2(z) = -(z^{-2} - b^2) / (1 - b^2 z^{-2})$, where $b^2 = 0.1380250$ in decimal arithmetic, is shown in FIGURE 14 to be as follows. The samples from the ADC **22** are delayed by two ADC sample clock durations in cascaded clocked delay elements **121** and **122**, for application as its first summand signal to a digital adder **123**. The sum output signal of the adder **123** provides the imaginary response from the filter **120**. The sum output signal of the adder **123** is delayed by two ADC sample clock durations in cascaded clocked delay elements **124** and **125**, for application to a digital adder **126** as its second summand signal. that receives the samples from the ADC **22** as its subtrahend input signal. The resulting sum output signal from the digital adder **126** is supplied as multiplier input signal to a digital multiplier **127** for multiplying a b^2 multiplicand signal, using a binary arithmetic. The resulting product output signal is applied to the digital adder **123** as its second summand signal.

FIGURE 15 shows a complex-signal filter resulting from modifying the FIGURE 14 complex-signal filter as follows. The position of the clocked delay element **118** is shifted so as to delay the sum output signal of the adder **113**, rather than to delay the digital output signal of the ADC **22**, and the digital output signal of the ADC **22** is applied to the node **119** without delay, thereby to cause real response to be provided at the output port of the shifted-in-position clocked delay element **118**. The real response provided at the output port of the shifted-in-position clocked delay element **111** is the same as the response provided at the output port of the clocked delay element **114**. So, the real response is provided from the output port of the clocked delay element **114** instead of from

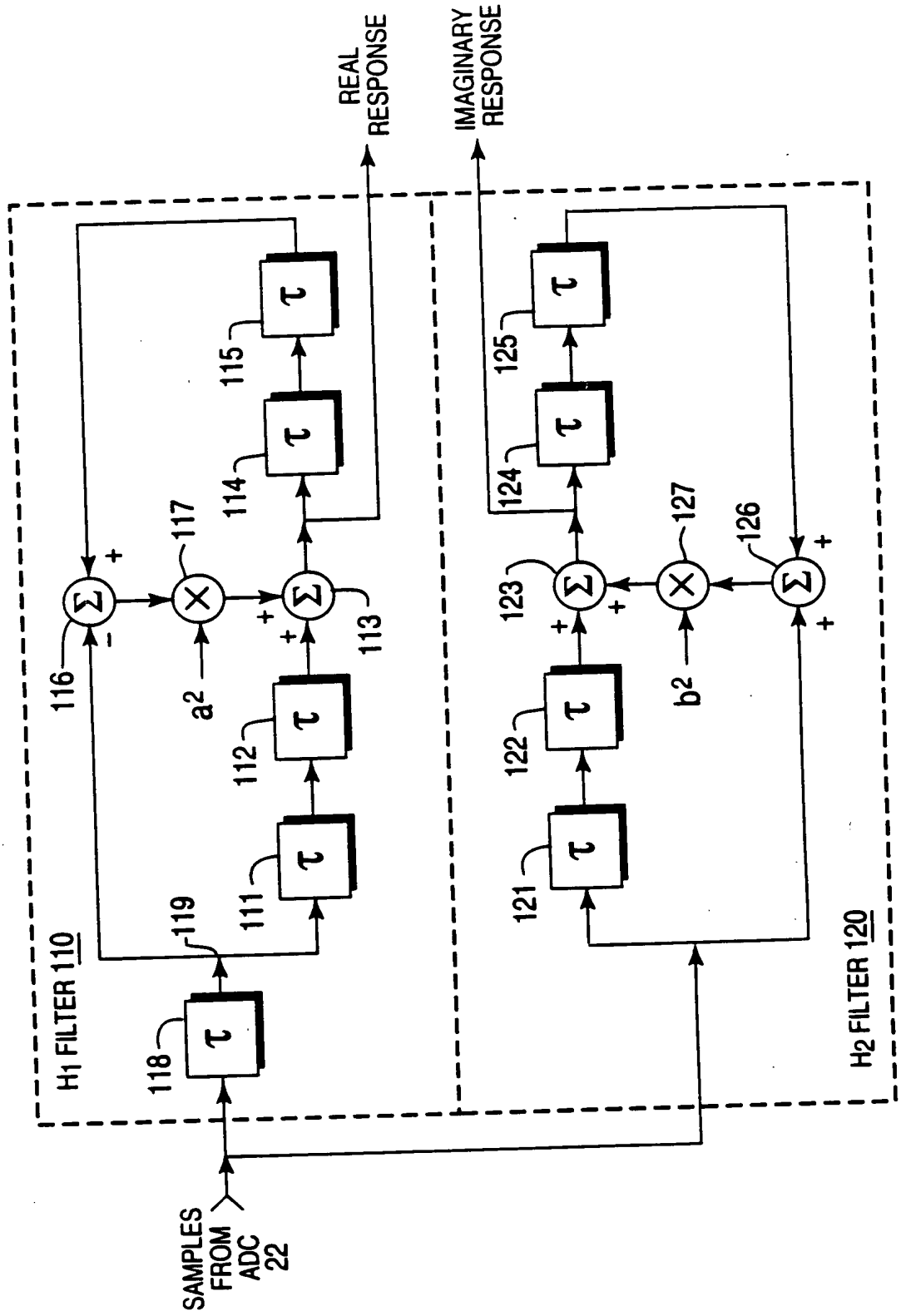
REAL RESPONSE
IMAGINARY RESPONSE
SAMPLES FROM ADC 22
H1 FILTER 110
H2 FILTER 120
118
119
111
112
113
114
115
116
117
a2
121
122
123
124
125
126
127
b2
τ
Σ
X

FIG. 14

#14

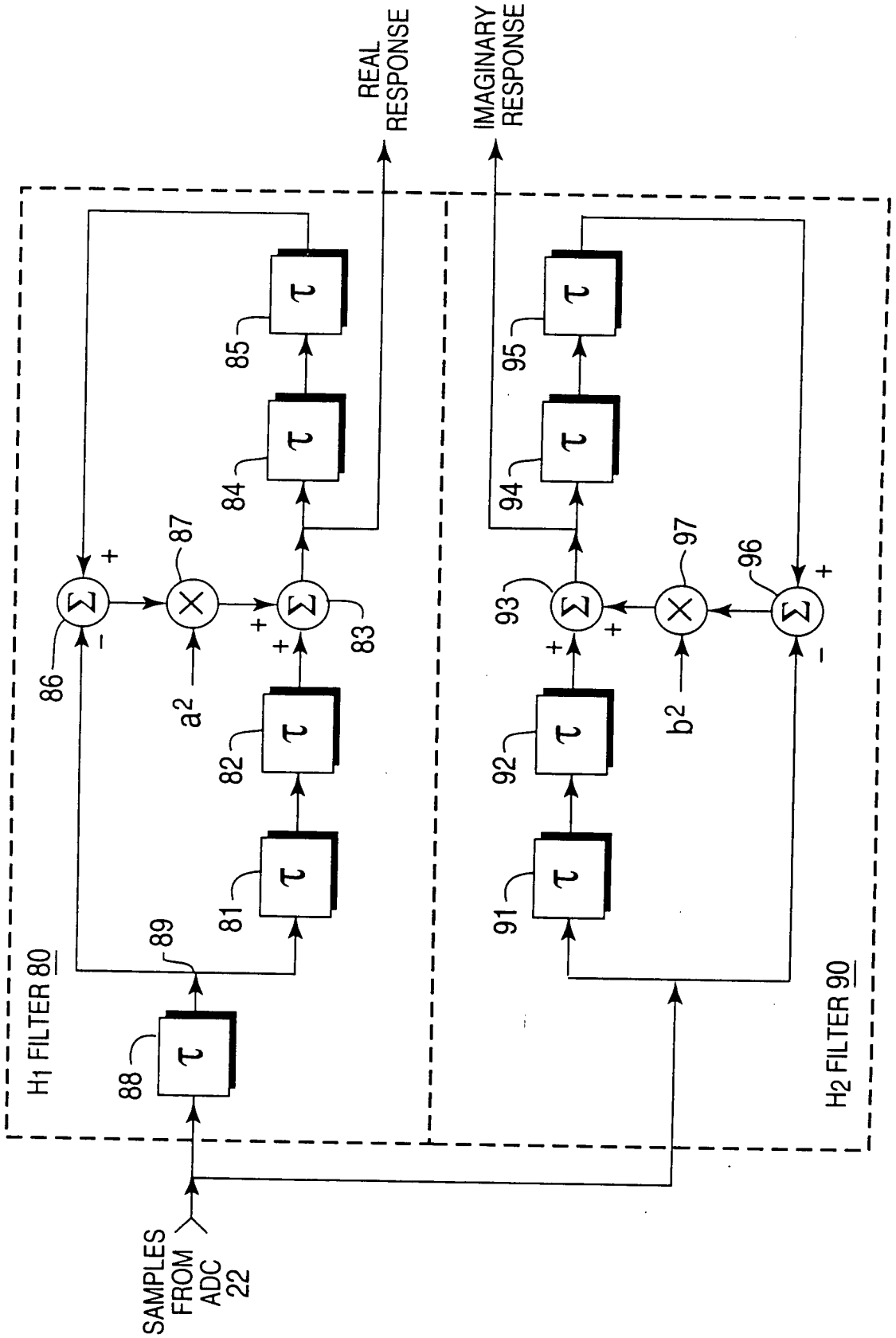
REAL RESPONSE
IMAGINARY RESPONSE
SAMPLES FROM ADC 22
H1 FILTER 80
H2 FILTER 90
88
89
81
82
83
84
85
86
87
a2
91
92
93
94
95
96
97
b2
τ
Σ
+
−
×

FIG. 7